Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A wireless receiver system comprising:

a receiver circuit that receives a wireless signal;

a demodulator coupled to the receiver circuit, the demodulator recovering a data signal and at least one clock signal from at least one signal output by the receiver circuit;

a computer configured to generate a read signal; and

a first-in first-out memory coupled to the demodulator to receive the data signal and the at least one clock signal, wherein the first-in first-out memory stores the data signal in response to the at least one clock signal, and wherein the first-in first-out memory is coupled to the computer to receive the read signal;

wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

2. (Currently Amended) The wireless receiver system of claim 1 wherein the read signal is synchronized with a computer clock signal.

3. (Canceled)

4. (Currently Amended) The wireless receiver system of claim 1 wherein the computer operates at a higher speed than the at least one clock signal.

5. (Currently Amended) The wireless receiver system of claim 5 wherein the computer reads the data signal from the first-in first-out memory in bursts.

6. (Currently Amended) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

7. (Currently Amended) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

8. (Currently Amended) The wireless receiver system of claim 1 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

9 - 13. (Canceled)

14. (Currently Amended) A method for receiving data comprising:

receiving a wireless signal;

recovering a data signal and at least one clock signal from the received wireless signal; and

storing the data signal into a first-in first-out memory in response to the at least one clock signal; and

providing, by a computer, a read signal to the first-in first-out memory;

wherein the computer reads the data signal from the first-in first-out memory without synchronizing a clock to the at least one clock signal.

15. (Previously Presented) The method of claim 14 wherein the read signal is synchronized with a computer clock signal.

16. (Canceled)

17. (Previously Presented) The method of claim 14 wherein the computer operates at a higher speed than the at least one clock signal.

18. (Previously Presented) The method of claim 14 wherein the computer reads the data signal from the first-in first-out memory in bursts.

19. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

20. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a length of data transmitted.

21. (Previously Presented) The method of claim 14 wherein the first-in first-out memory is sized in accordance with a product of a length of data transmitted and a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

22 - 27. (Canceled)

28. (New) A receiver system comprising:

a receiver adapted to receive a signal, generated in accordance with a transmit clock signal, to provide a data signal;

a first-in first-out memory coupled to the receiver to receive and store the data signal; and

a processing circuit coupled to the first-in first-out memory to retrieve the stored data signal in accordance with a read signal that is not synchronized to a clock signal derived from the transmit clock signal.

29. (New) The receiver system of claim 28 wherein the receiver recovers a clock signal from the received signal and the read signal is not synchronized to the recovered clock signal.

30. (New) The receiver system of claim 28 wherein the processing circuit comprises a data processor.

31. (New) The receiver system of claim 28 wherein the processing circuit comprises a host computer.

32. (New) The receiver system of claim 28 wherein the processing circuit is adapted to perform at least one of baseband processing, link management functions and protocol stack functions.

33. (New) The receiver system of claim 28 wherein the processing circuit reads the data signal from the first-in first-out memory in bursts.

34. (New) The receiver system of claim 28 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.

35. (New) A method for receiving data comprising:

receiving a signal, generated in accordance with a transmit clock signal, to provide a data signal;

storing the data signal into a first-in first-out memory; and

retrieving the stored data signal in accordance with a read signal that is not synchronized to a clock signal derived from the transmit clock signal.

36. (New) The method of claim 35 comprising recovering a clock signal from the received signal wherein the read signal is not synchronized to the recovered clock signal.

37. (New) The method of claim 35 wherein a processing circuit processes the retrieved data signal to perform at least one of baseband processing, link management functions and protocol stack functions.

38. (New) The method of claim 37 wherein the processing circuit comprises a host computer.

39. (New) The method of claim 37 wherein the processing circuit comprises a data processor and a host computer.

40. (New) The method of claim 35 comprising reading the data signal from the first-in first-out memory in bursts.

41. (New) The method of claim 35 wherein the first-in first-out memory is sized in accordance with a variation between a rate at which the first-in first-out memory is written and a rate at which the first-in first-out memory is read.